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10/543,173	07/22/2005	Masaki Yamada	274300US2PCT	7941

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EXAMINER	
CAVALLARI, DANIEL J	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
03/12/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/543,173	YAMADA ET AL.	
	Examiner	Art Unit	
	DANIEL CAVALLARI	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-12 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/22/2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the amendments submitted 12/29/2008. The amendments to claim(s) 1, 3, 4-12, 16, and new claims 17-19 are accepted.

Response to Arguments

Applicant's arguments filed 12/29/2008 have been fully considered but they are not persuasive.

In regard to the 112 second paragraph rejection, applicant's amendments clarify the ambiguity in regard to the undefined "system"; however they raise new issues as described below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-12, 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicant has used "series" and "parallel" to define the invention in the claims however the connections are not in "series" or "parallel" as stated in the claims. The well known definition of series is "A method of connecting circuits so that they share the same current" and a parallel connection is defined by connecting components so that they share the same voltage (see definitions illustrated below):

series connection A method of connecting components or circuits so that they share the same current, the voltage dividing between them depending on their impedance. See *Figure S.11*. The equivalent impedance Z_{eq} of a number of impedances Z_1, Z_2, Z_3, etc connected in series is given by

$$Z_{eq} = Z_1 + Z_2 + Z_3 + \text{etc.}$$

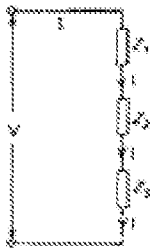


Figure S.11 A simple series circuit

parallel connection A method of connecting components or circuits so that they share the same voltage, the current dividing between the circuits depending on their impedance. See *Figure P.2*. The equivalent impedance Z_{eq} of a number of impedances Z_1, Z_2, Z_3, etc is given by

$$\frac{1}{Z_{eq}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{1}{Z_3} + \text{etc.}$$

but problems on impedances in parallel are probably best solved by use of the admittance concept, the equivalent admittance being the sum of the individual admittances thus:

$$Y_{eq} = Y_1 + Y_2 + Y_3 + \text{etc.}$$

See series connection.

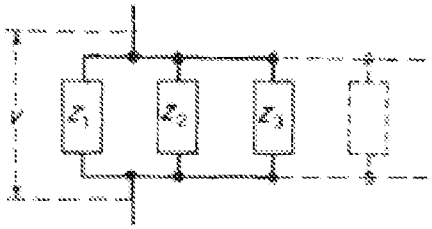
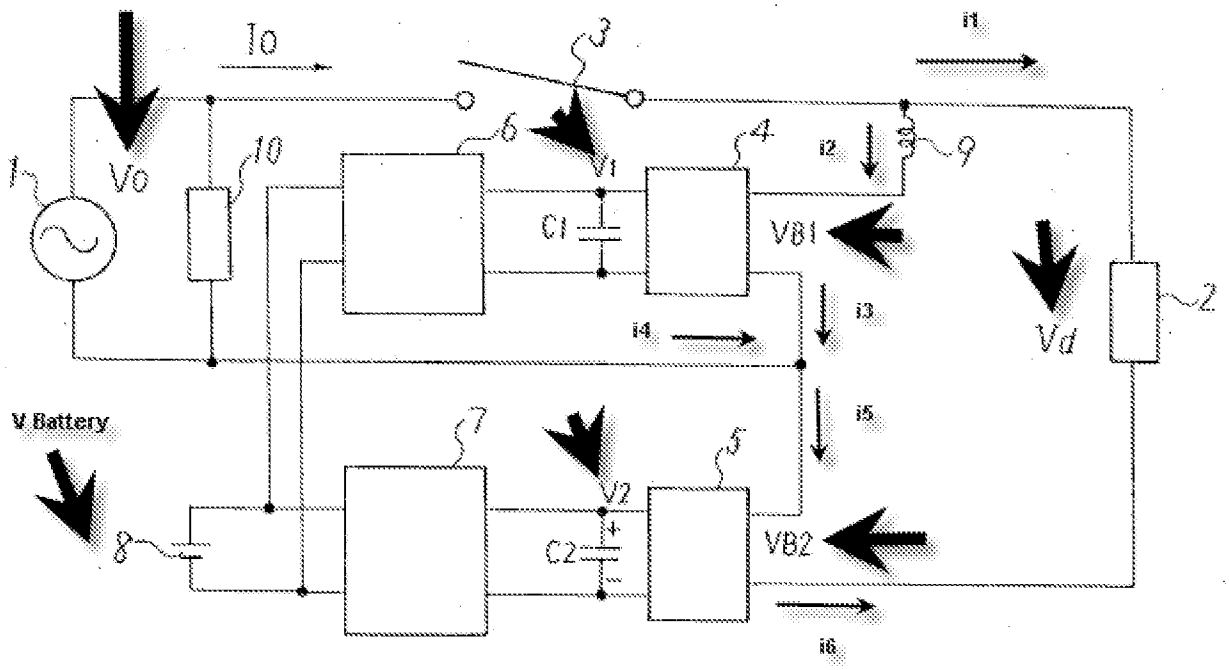


Figure P.2 Components connected in parallel have a common signal voltage V

Looking at applicant's invention (as shown in Figure 1 below), the provided connections cannot be defined as "parallel" and "series" as claimed. To highlight this point, the varying currents (represent by i1-i6) and voltages (voltages pointed out with the large arrows) which do not thereby meet the well known and established "parallel" and "series" connection definitions as defined in the art are illustrated (see definitions provide above).



In order to expedite and avoid piecemeal prosecution, **the following rejection is made to the extent that the claims are understood**, by considering those elements which are understood and interpreting their function in a manner which is consistent with the recited goals of the claims, and then applying the best available art.

The term “inverter/rectifier” is confusing and it is unclear whether the term is referring to “inverter and rectifier” or “inverter or rectifier”. The term will be examined as best understood as "inverter or rectifier".

It is noted switch operation is commonly reoffered to as "open" and “closed" and not "on" and "off" (wherein "on" and "off" is a condition of the load/controlled device).

In regard to claim 1

The claim states "to supply the electric power to the load by superimposing their output voltages" however it is unclear where the "superimposing" of output voltages occurs in applicant's invention. It appears that the "superimposing" occurs at the load itself and therefore the signals are not actually superimposed on each other but rather create a potential between the load (2) (see figure 1 above).

In regard to claims 5 and 19

The term "pseudo-sinusoidal voltage wave" is not one ordinarily used in the art to refer to a particular voltage waveform. The distinction between a "pseudo-sinusoidal voltage wave" and a real or actual pseudo-sinusoidal voltage wave is unclear. Therefore, the claim will be read on by any voltage waveform [noting that the issue was presented, but not addressed in the previous office action and further added in new claim 19].

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the particular interconnections of the converters (4, 5, figure 1) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Since the particular interconnection of the device is explicitly claimed, the drawings must provide an accurate representation of the invention incorporating the specific interconnections of

the converters (4-7). As the claims presently stand, the "series" and "parallel" connection provide the novel component of applicant's invention and are essential in understanding its operation. The present figures do not show the connections as claimed. If the claims are in fact accurate, then the figures should support the particular connections in the claims.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Keizo et al. (JP11-178216).

In regard to claim 1

A power supply apparatus comprising:

a straightforward switch (3, figure 1) which connects a power source (1) to a load (3), and supplying or interrupting an electric power served from the power source to the load [read on by opening and closing the switch];

a first single phase inverter (6);

a second single phase inverter (4); and

a battery (5) connected to direct current side terminals of said the first and second single phase inverters (see figure 1)

wherein said first and second single phase inverter/rectifiers are connected with the straight forward switch wherein when said switch is turned off (opened) to supply the electric power to the load by superimposing their output voltages (see Fig 1 and Abstract).

In regard to claims 5 and 14

Wherein the first and second single phase inverters form a pseudo- sinusoidal voltage wave comprising a voltage waveform having a plurality of output levels [noting that an alternating current alternates between a plurality of voltage levels) to output it to the load, by combining their output voltages (0 volts from inverter 6 and full voltage from inverter 4, figure 1) after decreasing in the system voltage and opening of the straightforward switch (see paragraph 7).

Claim 13

The power supply apparatus according to claim l, wherein said second single phase inverter is connected between said first single phase inverter and the power source (see figure 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, 12, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Oughton, Jr. (US 6,753,622).

In regard to claims 3, 7, and 18

Incorporating all arguments above, Keizo fails to teach either of the inverters connected to a DC-DC converter.

Oughton teaches a power supply system wherein an either the DC source (20) is connected to the inverter (822) via a DC-DC converter (824).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a DC-DC converter between the battery and inverter as taught by Oughton into the system of Keizo. The motivation would have been to better regulate the battery voltage and given the system flexibility with the ability to power the system with a battery voltage different than the DC operating voltage

In regard to claim 12

Keizo further teaches:

wherein the direct current voltage of said second single phase inverter is changed by said DC-DC converter according to an amount of decreased or increased system voltage (see paragraph 5).

In regard to claim 19

Keizo further teaches:

Wherein the first and second single phase inverters form a pseudo- sinusoidal voltage wave comprising a voltage waveform having a plurality of output levels [noting that an alternating current alternates between a plurality of voltage levels) to output it to the load, by combining their output voltages (0 volts from inverter 6 and full voltage from inverter 4, figure 1) after decreasing in the system voltage and opening of the straightforward switch (see paragraph 7).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Ozawa (US 5,866,506).

Incorporating all arguments above, Keizo fails to explicitly teach superimposing different voltages at the load to provide the drive for the load. Ozawa teaches superimposing different voltages at the load creating a drive voltage (See figure 5B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide different voltages at the load from the inverters of Keizo as taught by Ozawa. The motivation would have been to provide the load with a drive voltage (noting that if the voltage provided is the same voltage (potential) then there is no drive voltage and no power or drive to operate the load).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Sakai (US 6,034,514).

Keizo teaches the second inverter equalizing harmonic current but fails to explicitly teach the converter superimposing voltage for compensation by pulse width modulation or voltage value. Sakai teaches a power supply apparatus wherein pulse width modulation is used to adjust for voltage fluctuations (see Column 3, line 55 to column 4, line 11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the PWM technique for adjusting for fluctuations as taught by Sakai into the system of Keizo. The motivation would have been to use a well known and established method of voltage control to compensate for fluctuations in the voltage.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. (hereinafter referred to as Keizo) in view of Bong-Hwan et al. ("Improved Single-Phase Line-Interactive UPS).

Incorporating all arguments above, Keizo teaches a switch (2, figure 1) but fails to explicitly teach what the switch is made of. Bong-Hwan et al. (hereinafter referred to as Bong-Hwan) teach a power supply apparatus comprising a semiconductor switch (see "bypass switch", figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the semiconductor switch taught by Bong-Hwan in place of the switch taught by Keizo. The motivation would have been to use a switch well known and readily available.

Claims 8-11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. in view of Vinciarelli et al. (US 5,786,992) (hereinafter referred to as Vinciarelli).

In regard to claim 8

Incorporating all arguments above, Keizo fails to explicitly teach inverters connected in series. However, Vinciarelli teaches connecting converters in series in order to reduce the minimum operating voltage (see column 3, lines 10-18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the series connected converter configuration as taught by Vinciarelli in the design of the inverters taught by Keizo. The motivation would have been to reduce the minimum operating voltage.

In regard to claim 9

Vinciarelli further teaches a plurality of converters connected in series with attached DC sources (capacitors, see figure 15) however Keizo and Vinciarelli fail to explicitly teach the DC sources comprising a voltage relationship of 1:2, or 1:3.

However, it would have been an obvious matter of design choice to size the sources in a 1:2 or 1:3 voltage relationship, since such a modification would have involved a mere change in size of a component and change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

In regard to claims 10 and 16

Keizo further teaches compensating for reactive power (See abstract).

In regard to claim 11

Vinciarelli further teaches a plurality of converters connected in series with attached DC sources (capacitors, see figure 15) however Keizo and Vinciarelli fail to explicitly teach said second inverter having a DC voltage 0.5 or more of the DC voltage of the single phase inverter generating the least voltage out of a plurality of the inverters constituting the first single phase inverter.

However, it would have been an obvious matter of design choice to size the sources in a 1:2 or 1:3 voltage relationship, since such a modification would have involved a mere change in size of a component and change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Keizo et al. in view of Vinciarelli et al. (US 5,786,992) (hereinafter referred to as Vinciarelli) in further view of Shibata (US 5,570,004).

Incorporating all arguments above, Keizo teaches opening said switch when an abnormal system voltage drop is detected (see translation, paragraph 9) however fails to explicitly teach a detector used to open/close said switch (although a detector is inherent in said operation).

Shibata teaches a voltage drop detector configured to detect if a system voltage from said power source abnormally drops in magnitude, and open said switch when an abnormal system voltage drop is detected.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the voltage drop detector taught by Shibata with the power supply apparatus taught by Keizo. The motivation would have been to provide a known voltage detector with the predictable result of controlling the switch wherein Keizo is silent in regard to the particular circuitry used.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the

THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Cavallari whose telephone number is 571-272-8541. The examiner can normally be reached on Monday-Friday 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571)272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel Cavallari/

March 5, 2009

/Albert W Paladini/
Primary Examiner, Art Unit 2836 3/6/09